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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,566	06/28/2001	Baruch Solomon	2207/10607	2824

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KENYON & KENYON
1500 K STREET, N.W., SUITE 700
WASHINGTON, DC 20005

EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,566	SOLOMON ET AL.Y	
	Examiner	Art Unit	
	Gary J Portka	2188	

-- The MAILING DATE of this communication appears on the c ver sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,10-15 and 27-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6 and 10-15* is/are allowed.

6)☒ Claim(s) *27,29-36, and 39-41* is/are rejected.

7)☒ Claim(s) *28,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/16/04,11/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 22, 2004 has been entered. Claims 1-6 and 10-15 have been amended, and claims 27-41 have been added by Applicant. Claims 1-6, 10-15, and 27-41 are pending.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on November 22, 2004 and August 16, 2004 were considered by the examiner.

Claim Objections

3. Claims are objected to because of the following informalities: Claim 27 recites at the last line "terminating the foregoing operations of the instruction processing system", upon the condition that the "address hits the micro-instruction cache". Since the "foregoing operations" depend upon the address hitting the instruction processing system, the claim language appears to require that the address hit both if it hits the micro-instruction cache. Claim 31 similarly recites at the last line "terminating the outputting, and converting operations of the second cache" if the address hits the first cache, but likewise those operations can only be terminated if they are started, which

requires the address also hitting the second cache. Examiner questions whether these are the desired interpretations.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 32-34, and 39-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 32 recites "the instruction processing system" which lacks proper antecedent basis. Claim 33 recites "the micro-instruction cache" and "the instruction cache" which lack proper antecedent basis. Claim 34 recites "the addressed micro-instructions", "the micro-instruction cache" (2 places), and "the instruction processing system", which lack proper antecedent basis. Claim 39 recites a "cache lookup unit" and a "cache fetch unit", wherein the independent claim 35 recited a "cache lookup unit" and a "data fetch unit". It cannot be determined whether it is intended to have two cache lookup units, a cache fetch unit, and a data fetch unit, or only one cache lookup unit and one fetch unit. Claims 40-41 incorporate this limitation by dependency.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 31, 33, 35-36, 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Friendly et al., "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism".

8. As to claim 31, Friendly discloses a method comprising applying an address in parallel to first and second caches (at PC), if the address hits the second cache (the instruction cache) outputting addressed data therefrom and converting it to a format of the first cache (since the instructions are decoded), and if the address hits the first cache, outputting addressed data therefrom and terminating the outputting and converting operations of the second cache (via the Trace Cache Miss signal at the pass gate shown below the Decoder, Fig. 1, see also sections 2 and 3; the gate effectively terminates operations of the circuit above it).

9. As to claim 33, the Trace Cache Miss signal is the disabling output signal.

10. As to claim 35, Friendly discloses a system comprising processor for performing instruction pre-processing and to output decoded instructions, comprising UOP cache (Trace Cache) and instruction cache having inputs coupled to a common addressing input (at PC), the UOP cache having out hit/miss indicator (Trace Cache Miss) to selectively disable the instruction cache (at the pass gate shown below the Decoder, Fig. 1, see also sections 2 and 3; passing of the signal at the gate effectively enables the circuit above it), and execution unit (MPS Execution Core) to receive and execute the decoded instructions from the processor. The instruction cache further has a cache

lookup unit and a data fetch unit (i.e., a tag array and a data array), which are by definition elements of a cache.

11. As to claim 36, memory to store and retrieve data associated with the instructions is inherent, or may be considered registers of the execution core.

12. As to claim 39, Friendly has a cache lookup unit and a cache fetch unit (i.e., a tag array and a data array), which are by definition elements of a cache, and coupled to the hit/miss indicator via the pass gate.

13. Claims 27 and 31 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art.

14. As to claim 27, the admitted prior art of paragraph 2 and Fig. 2 discloses an address provided in parallel to a micro-instruction cache (170) and an instruction processing system (140, 150, 160, and 180), if the address hits the instruction processing system outputting addressed data from an instruction cache (at 140) performing instruction synchronization (at 150), and decoding instructions obtained therefrom (at 160), and if the address hits the micro-instruction cache, outputting addressed micro-instructions therefrom, and terminating the operations of the instruction processing system (inherent since the express purpose of utilizing the UOP cache is to avoid if possible the latency involved with accessing un-decoded instructions via the instruction cache).

15. As to claim 31, the admitted prior art of paragraph 2 and Fig. 2 discloses an address provided in parallel to first (170) and second (140) caches, if the address hits the second cache outputting addressed data therefrom (at 140) converting the output

data to a format of the first cache (at 180), and if the address hits the first cache, outputting addressed data therefrom, and terminating the operations of the second cache (inherent since the express purpose of utilizing the UOP cache is to avoid if possible the latency involved with accessing un-decoded instructions via the instruction cache).

16. Claim 31 is rejected under 35 U.S.C. 102(a) as being anticipated by Jourdan, et al., "extended Block Cache".

17. As to claim 31, Jourdan discloses an address provided in parallel to first (TC) and second (instruction) caches, if the address hits the second cache outputting addressed data therefrom, converting the output data to a format of the first cache ("builds mode", see last paragraph of section 2.3), and if the address hits the first cache, outputting addressed data therefrom ("delivery mode"), and terminating the operations of the second cache (understood since an express purpose of utilizing the TC is to avoid if possible the latency involved with accessing un-decoded instructions via the instruction cache).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Friendly et al., "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", in view of the admitted prior art.

20. As to claim 27, Friendly discloses a method comprising providing an address in parallel (at PC) to a UPO cache (Trace Cache) and an instruction processing system (right side of Fig. 1), if the address hits the instruction processing system outputting the addressed data from an instruction cache and decoding instructions obtained therefrom and if the address hits the micro-instruction cache, outputting addressed micro-instructions therefrom, and terminating the operations of the instruction processing system (via the Trace Cache Miss signal).

Friendly does not disclose performing instruction synchronization of the output from the instruction cache. However, Applicant has admitted at paragraph 2 and at Fig. 2 of the present Application, that instruction synchronization was used in the prior art in order to allow for instructions of varying lengths. An artisan would have desired to avoid restricting instructions to fixed lengths and thus would have been motivated to use the instruction synchronization of the prior art in order to be able to use variable length instructions. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the recited instruction synchronization, because this was a known means of allowing for variable length instructions.

21. As to claim 29, the Trace Cache Miss signal is the disabling output signal.

22. Claims 34, 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Friendly et al., "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", in view of Sheppard et al., U.S. Patent 5,913,223.

23. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Friendly et al., "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", in view of Sheppard et al., U.S. Patent 5,913,223, and further in view of the admitted prior art.

24. As to claim 40, Friendly discloses the invention substantially as described above with regard to claims 1-4 and 10-13. Friendly does not disclose the UOP cache comprising a delay element between the lookup unit and data fetch unit. However, Sheppard teaches that power consumption of a cache may be reduced by delaying access of a data unit until it is known if there is a hit via the lookup unit. See Sheppard Abstract, col. 3 lines 59-67, col. 4 line 63 to col. 5 line 2, col. 5 lines 33-39, and col. 6 lines 61-67. Sheppard therefore shows the motivation for adding a delay between the lookup unit and data fetch unit as recited. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a delay element between the lookup unit and the data fetch unit, because this was a known means of reducing power consumption of a cache.

25. As to claims 30, 34, and 41, the additional limitation of delay corresponding to a processing time of the instruction processing system is inherent to the extent recited (the delay indeed may be considered to influence the processing time); the delay

element is controlled by the hit/miss indicator to the extent that only upon a hit will the delay element forward to address to the next stage.

Allowable Subject Matter

26. Claims 1-6 and 10-15 are allowed.

27. Claims 28 and 37-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, as well as amended to overcome objections made above.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

January 9, 2005